T-COM Corporation
Digital Telephony Instrumentation

INSTRUCTION MANUAL

DS1/PCM TEST GENERATOR

MODEL 515A

Instrument S/N : 515A____

Instruction Manual No. : IM515A01

T-COM Corporation

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WARRANTY

T-COM PRODUCTS ARE WARRANTED AGAINST DEFECTS IN MATERIALS AND WORKMANSHIP FOR ONE YEAR FROM THE DATE OF SHIPMENT. OUR OBLIGATION IS LIMITED TO REPAIRING AND REPLACING PRODUCTS THAT PROVE TO BE DEFECTIVE DURING THE WARRANTY PERIOD AS A RESULT OF NORMAL AND INTENDED USE OF THE PRODUCT. THIS WARRANTY DOES NOT APPLY TO DEFECTS RESULTING FROM MISUSE, NEGLIGENCE, ACCIDENTS OR UNAUTHORIZED REPAIRS OR MODIFICATIONS.

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Notes:

- With the exception of transportation costs, there is no charge for repair of instrument under warranty.

- Estimates of charges for non-warranty or other service work will always be supplied, if requested, before work begins.

Please help us keep you informed! So that we may send you future applications notes and manual updates, please complete and return the Warranty Registration Card below. Your cooperation is appreciated.

WARRANTY REGISTRATION CARD

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1. GENERAL INFORMATION

1.1 SCOPE

This instruction and operation manual contains information to install and to operate the T-COM model 515A DS1/PCM Simulator.

1.2 INTRODUCTION

The model 515A is a multi-purpose PCM test generator designed to facilitate the testing and troubleshooting as well as development of T-carrier transmission and digital switching systems interfacing with DS1 formatted bit streams.

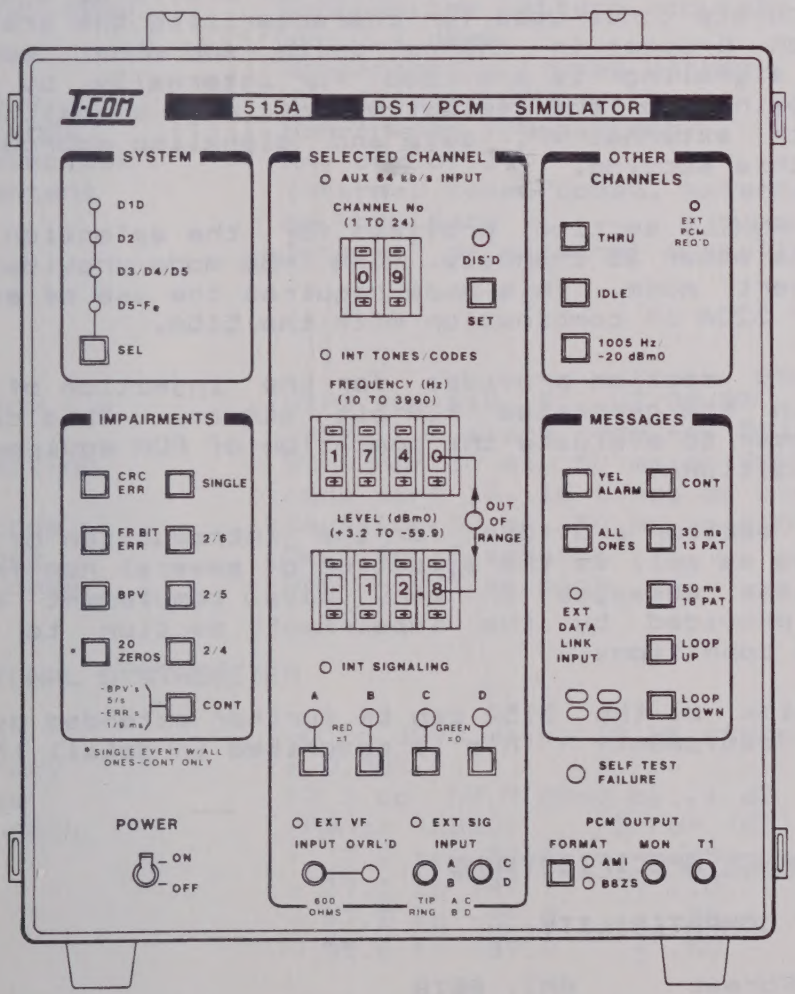


Figure 1.1 Front Panel

The set capabilities are primarily grouped into four sections operating in combination. These sections are:

- SELECTED CHANNEL
- OTHER CHANNELS
- IMPAIRMENTS
- MESSAGES

The PCM bit stream selection provides primarily for framed PCM transmission. However, some limited unframed PCM generation is also provided for convenience. The framed transmission is compatible with D1D, D2, D3, D4 and D5/Fe channel bank formats.

The SELECTED CHANNEL section provides for selecting the VF and out of band signaling content of one channel. Internal selection includes a digital tone/code synthesizer providing a wide range of highly accurate tones used for characterizing the transmission and conversion process in channel units and other subsystems. Out of band signaling is provided for internally by a set of switches allowing for the selection of any signaling state. Interface with external VF, data and signaling sources is also provided by this section.

The OTHER CHANNELS section provides for the selection of the content of the other 23 channels. The THRU mode provides for the 'Drop-and-Insert' mode. This mode requires the use of either the T-COM 220A or 320A in combination with the 515A.

The IMPAIRMENTS section provides for the injection of specific impairments in the generated PCM bit stream. This capability enables the user to evaluate the operation of PCM equipment under non-ideal conditions.

The MESSAGES section provides for the introduction of data and alarm messages as well as the selection of several non-framed PCM signals. These messages in many ways complement the test capabilities provided by the impairment section to simulate specific test conditions.

The capabilities of the 515A can be further extended by the use of auxiliary equipment. This is described in detail in chapter 3.

1.3 PERFORMANCE SPECIFICATIONS

SYSTEM FORMAT COMPATIBILITY

Transmission Format	AMI, B8ZS
Channel Bank	D1D, D2, D3, D4, D5 and D5/Fe

PCM DIAGNOSTIC CHARACTERISTICS

Clock Rate	Internal 1,544,000 ± 30 Hz External 1,544 ± 40 kHz
T1 Output Level	3.0 V ± 10% when terminated with a 100 ohm resistor
Mon Output Level	.31 V ± 10% when terminated with a 100 ohm resistor

PCM SIGNAL SELECTION

Idle	11111111 code per channel
1005 Hz/ -20 dBm0	Synthesized pattern accurate to 1.0 Hz and 0.1 dBm0
All ones	Non-framed all-ones pattern
Loop-up code	Non-framed 10000 pattern
Loop-down code	Non-framed 100 pattern
Channel selection	Any one of 24
Channel content	Internal tones/codes, external VF or 64 kb/s data Internal or external signaling

MESSAGES

Yellow alarm	B2=0 for D1D, D2, D3/D4/D5 Data link alarm code for D5/Fe
Alarm selection	B2=0 for 30 ms, 50 ms or CONT. Alarm code sent 13, 18 times or continuously
All ones code	Sent for 30 ms, 50 ms or continuously
Loop-up code	Sent for 5 seconds
Loop-down code	Sent for 5 seconds

DIGITAL SIGNAL SYNTHESIZER

Freq range	10 to 3990 Hz by 10 Hz steps
Freq accuracy	+ 0.38%
Level range	+3.2 to -59.9 dBm0 by .1 dB
Level accuracy	Range (dBm0) Error (dB) + 3.2 to -39.0 ± .05 - 39.1 to -47.7 ± .10 - 47.8 to -55.5 ± .20 - 55.6 to -59.9 ± .50

VF SIGNAL ENCODER

Input level	+3 to -55 dBm0
Input impedance	600 ohm balanced
Return loss	≥ 28 dB / 300 Hz to 3000 Hz
Freq response	Within ± .15 dB / 300 to 3000 Hz
(referred to 1010 Hz)	Within +.3 & -1.0 dB / 200 to 3300 Hz

	Min 20 dB loss at 60 Hz	
Quantizing distortion	Level (dBm0)	S/D ratio (dB)
(C-message weighted)	0 to -20	$\geq$ 35
	-21 to -30	$\geq$ 32
	-31 to -40	$\geq$ 27
	-41 to -45	$\geq$ 23
Gain tracking error	Level (dBm0)	Error (dB)
	-10 to -35	$\leq$ .25 dB
	-36 to -50	$\leq$ .50 dB
Encoder noise	$\leq$ 18 dBrnC0	
Overload indicator	Level threshold 3.4 $\pm$ .2 dBm0	

SIGNALING

Internal selection	States A, B, C and D set to 0 or 1 by individual switches
External control	Contact closure to sleeve (GND) or TTL state Low=1 Open contact or TTL state high=0

64 kb/s DS0 ACCESS (Option 01)

Data Input	Logic mode TTL level compatible
Timing clocks	8 KHz pulse coincident with bit 8 64 KHz with 5/8 duty cycle TTL level compatible

IMPAIRMENTS

BPV	Single and at rate of 5/sec
FR BIT ERR	Single, 2/6, 2/5, 2/4, and at rate of 110/sec
CRC ERR	Single and at rate of 110/sec (in D5-Fe mode only)
20 ZEROS	20 consecutive zeros with all ones pattern only

EXTERNAL REAR PANEL ACCESS (25 POS. D-SUB CONNECTOR)

All inputs are CMOS logic level compatible

Clock	50% duty cycle on BNC connector
Data link access	4 KHz clock and data input

220A/320A interface provides for drop-and-insert mode

MISCELLANEOUS

AC powering	108-126 VAC 60 Hz 10W
Operating temp	10 to 40°C (50 to 104°F)
Storage temp	-30 to 70°C (-22 to 158°F)
Humidity	Up to 90% non-condensing

Dimensions	10.5" (H) X 8.5" (W) X 8.5" (D) (D=10" with front cover)
Weight	9.5 Lbs (4.3 Kg) with option 515A-01

ORDERING INFORMATION

Model 515A includes:	Basic instrument Front cover 6 foot AC power cord One operation manual
Option 515A-01	Provides 64 kb/s DSO interface compatible with WECO's KS 20909 and Telepath Inc.'s TPI 109A

ACCESSORIES:

1886-003	Canvas carrying case
1886-004	Polyethylene shipping case
1690-001	4 foot patch cord terminated with miniature plugs
1690-002	4 foot patch cord terminated with miniature and 310 type plugs
1694-001	Miniature to 310 adapter plug
2700-014	Interconnecting cable to 220A/320A (required for drop-and-insert)
IM515A01	Extra instruction manual

REPLACEMENT PARTS:

1700-012	Power cord
1500-006	Fuse .20A Fast Blow
2751-044	Front cover assembly

2. INSTALLATION

2.1 INTRODUCTION

This section contains information and instructions for installing the model 515A. Included are procedures for initial inspection, preparation for use and repacking for shipment.

2.2 INITIAL INSPECTION

Inspect the shipping container for damages. Should any damage be found, the container must be kept until all contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in section 6. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify your T-COM Representative.

If the shipping container is damaged, notify the carrier as well as the Representative. Keep the shipping material for the carriers' inspection.

2.3 PREPARATION FOR USE

Powering -- The model 515A operates from the 120 VAC line.

Powering is accomplished by connecting the 120 VAC via the six-foot, three conductor AC cord supplied with the 515A to the AC inlet located on the left side of the 515A.

CAUTION

1. Removal of the ground pin from the supplied AC power cord constitutes a safety hazard and voids the warranty.

2. The AC Line voltage must be in the range of 110-125 VAC for proper operation. Operation of the 515A when the Line voltage is outside this range may cause permanent damage to the set.

The set is ready to use when connected to the line.

2.4 REPACKING FOR SHIPMENT

The use of the original shipping carton and packing material is highly recommended. If the original packing material is not

available, you may use any strong container. Wrap the instrument in heavy paper or a plastic bag and surround it with three or four inches of shock absorbing material to cushion it firmly and prevent movement inside the container.

Note: Your authorized T-COM representative is ready to assist you in any situation and you are always welcome to directly contact the T-COM service department:

Customer Service
T-COM
805 East Middlefield Road
Mountain View, CA 94043
(415) 964-3415

All equipment returned to the factory must be accompanied by a manufacturer's Return Authorization number. In order to get an RA number, customers should call in or write, with the model and serial numbers of equipment to be returned, PRIOR to shipment. A number will be issued, which will be referenced in both the packing slip and the purchase order associated with the equipment. To ensure that the instrument is satisfactorily repaired, include with the instrument a comprehensive description of the problem(s) encountered.

3. OPERATION

3.1 INTRODUCTION

This section provides operating information, explains the functions of the 515A controls, connectors and indicators and describes measurement capabilities of the instrument.

3.2 FRONT PANEL FEATURES

The 515A front panel features are described below. The description numbers match the numbers in figure 3.1.

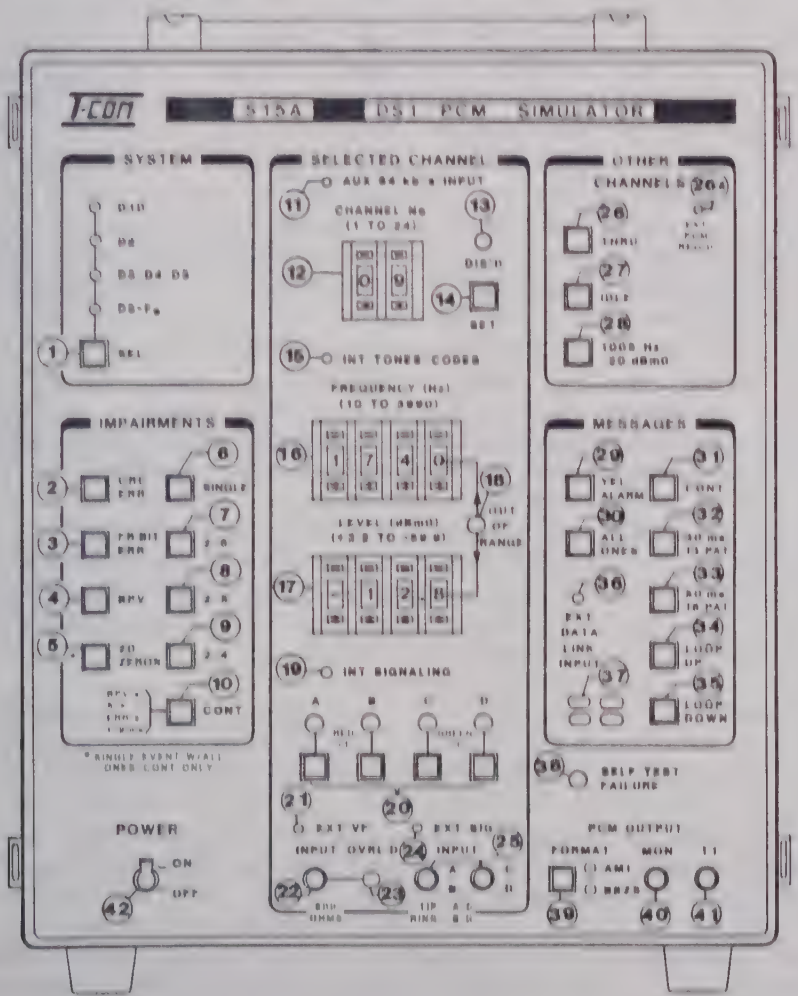


Figure 3.1 Front Panel Features

System Section

1 SEL -- Repeated depression of this key causes the successive selection of the channel numbering sequence and framing format associated with the D1D, D2, D3/D4/D5 and D5-Fe channel banks. A single audible beep accompanies each depression of this switch. This switch does not change the framing format when the set operates in the THRU mode.

Selected Channel Section

11 AUX 64 kb/s INPUT -- This LED is turned on when a plug is inserted in the rear panel mounted DS0 Data input jack associated with option 515A-01. When this LED is on, the full content of the channel is controlled by the externally applied 64 kb/s data, and all other LED's in this section are turned off with the possible exception of DIS'D (13).

12 CHANNEL NO. -- This switch selects any one of the 24 channels in the DS1 bit stream. When a non-existent channel number is selected, (i.e., 30) the selection is invalid.

13 DIS'D -- This LED indicates, when lit, that the CHANNEL NO. selection (12) is disabled. This results when a non-existent channel number is selected, when a change in the channel selection takes place while in the THRU mode (see OTHER CHANNELS section), or when an unframed bit stream is being generated.

14 SET -- This key is used only when a new channel selection must be enabled when in the THRU mode. If the depression results in enabling the selection, the DIS'D LED (13) turns off and a single audible beep is delivered.

15 INT TONES/CODES -- This LED is turned on if no plug is inserted in the DS0 data input jack or in the EXT VF input jack (22). When lit, the VF content of the selected channel number is that selected by the digital tone synthesizer controlled by switches 16 and 17.

16 FREQUENCY -- This switch selects the frequency of the synthesized digital tone. This frequency can be set in the range of 10 Hz to 3990 Hz by discrete increments of 10 Hz.

17 LEVEL -- This switch selects the level of the synthesized digital tone. This level can be set in the range of +3.2 to -59.9 dBm0 by steps of .1 dB.

18 OUT OF RANGE -- This LED is lit when the FREQUENCY (16) and/or LEVEL (17) selections are set outside of their respective range. In this case the content of the selected channel is the idle code (11111111).

19 **INT SIGNALING** -- This LED is turned off when a plug is inserted into the rear panel DS0 input jack or into either EXT SIG input jack (25).

20 **A, B, C, D** -- When the INT SIGNALING mode prevails each switch selects the state of the corresponding signaling bit; repeated depression of each key causes toggling of the states. The selected state is identified by the color of the LED: red for state 1, green for state 0. When the system selection is D5-Fe signaling bits, C & D are active, otherwise the LED's for bits C & D are off.

21 **EXT VF** -- This LED is lit when a plug is inserted in jack 22 and no plug is inserted in the rear panel DS0 input jack. When this LED is lit, the VF content of the selected channel number is the encoded externally applied VF signal.

22 **EXT VF INPUT** -- This jack provides a 600 ohm input impedance to the externally applied VF signal source. The input is balanced and insulated from the instrument ground.

23 **OVRL'D** -- This LED is lit when the externally applied VF signal exceeds the maximum encoding level : nominally 3.2 dBm0.

24 **EXT SIG** -- This LED is lit when a plug is inserted in jacks 25 and no plug is inserted in the rear panel DS0 input jack. When this LED is lit, the out of band signaling content of the selected channel is the externally applied signaling at jacks 25.

25 **EXT SIG INPUT** -- These two jacks provide for the external access of bit A & B and C & D respectively. Closure to ground of the tip or ring of either jack causes the state 1 to be introduced in the corresponding bit. The left side jack accesses bits A and B on tip and ring, respectively. The right side jack accesses bits C and D on tip and ring, respectively.

Other Channels

26 **THRU** -- This switch selects the THRU mode. Entry into this mode is conditioned on the active connection between the 515A and either the T-COM 220A or 320A via the rear panel mounted 25 position connector. If the connection is not established or the other set is not turned on, an attempt to enter in the THRU mode results in a double audible beep and the flashing of 26a. When the THRU mode prevails, the PCM bit stream delivered by the 515A is identical to that monitored by the T-COM 220A or 320A on Line 1/DG1 except for the content of the selected channel if not disabled. The THRU mode is indicated by the lit LED in the THRU switch.

Exit from this mode requires to first depress the THRU key, and within 700 ms depress either the IDLE (27) or the 1005 Hz/-20 dBm0 (28) key.

27 **IDLE** -- When this selection prevails, as indicated by the lit LED in the switch, the idle code (11111111) is inserted into every channel except for the selected channel unless disabled. Entry into this mode from the 1005 Hz/-20 dBm0 is by simple depression of the IDLE key. For entry from the THRU mode refer to item 26 above.

28 **1005 Hz/-20 dBm0** -- When this selection prevails as indicated by the lit LED switch, a synthesized digital tone of 1005 Hz at a level of -20 dBm0 is inserted into every channel except for the selected channel unless disabled. Entry into this mode from the IDLE mode is by simple depression of the 1005 Hz/-20 dBm0 key. For entry from the THRU mode refer to item 26 above.

Messages

29 **YELLOW ALARM** -- When this switch is depressed a latent selection is made as indicated by the lit LED in this switch. Actual insertion of the alarm code takes place when keys 32 or 33 are depressed or when key 31 is lit. The yellow alarm code cannot be introduced in the bit stream delivered by the 515A when the THRU mode prevails. The yellow alarm code differs according to the system selection 1. When D1D, D2, or D3/D4/D5 is selected, this code consists in forcing the state of the second most significant bit in each channel to zero. When D5-Fe is selected, this code consists of a repeated sequence of 8 consecutive 1 bits followed by 8 consecutive 0 bits carried by the data link.

30 **ALL ONES** -- When this switch is depressed a latent selection is made as indicated by the lit LED in this switch. Actual introduction of the ALL ONES code in the generated bit stream takes place when keys 32 or 33 are depressed or when key 31 is lit.
The ALL ONES code cannot be introduced in the bit stream delivered by the 515A when the THRU mode prevails. The ALL ONES code is devoid of framing information, and while it is being sent the channel selection is disabled and all LED's in the OTHER CHANNELS section are turned off.

31 **CONT** -- When legitimately depressed, this key lets either the YEL ALARM (29) or the ALL ONES (30) condition prevail in a continuous manner. This is indicated by the lit LED in the switch. To exit this mode, depress either CONT, key 32 or key 33. This mode applies only to the YEL ALARM or ALL ONES.

32 30 ms/13 PAT -- When legitimately depressed this key lets either the YEL ALARM or the ALL ONES condition prevail for 30 milliseconds. If the system selection is D5-Fe and the YEL ALARM is selected, 13 patterns of the alarm code are sent following the depression of the 30 ms/13 PAT key.

33 50 ms/18 PAT -- When legitimately depressed this key lets either the YEL ALARM or the ALL ONES condition prevail for 50 milliseconds. If the system selection is D5-Fe and the YEL ALARM is selected, 18 patterns of the alarm code are sent following the depression of the 50 ms/18 PAT key.

34 LOOP-UP -- When legitimately depressed this key results in introducing the remote loop-up code (1000010000..), for 5 seconds, in the generated bit stream. This code contains no framing information, and while sent, the channel selection is disabled and all LED's in the OTHER CHANNELS section are turned off.
When in the THRU mode this code cannot be sent.

35 LOOP-DOWN -- When legitimately depressed this key results in introducing the remote Loop-down code (100100100..) for 5 seconds in the generated bit stream. This code contains no framing information, and while sent, the channel selection is disabled and all LED's in the OTHER CHANNELS section are turned off.
When in the THRU mode this code cannot be sent.

36 EXT DATA LINK INPUT -- This LED provides indication of the selection of the external data link input message. This LED can be lit only when the D5-Fe mode is selected and pin 16 on the rear panel mounted 25 position connector is grounded. When the YEL ALARM code is being sent the EXT DATA LINK INPUT LED is momentarily turned off since the datalink is then preempted to carry the ALARM code.

37 ACOUSTIC BEEPER -- A single audible beep indicates a legitimate key entry. A double audible beep indicates an illegitimate request (normally accompanied by the flashing of one or more LED's indicating the reason for rejection).

Impairments

2 CRC ERR -- When this switch is legitimately depressed a latent selection is made as indicated by the lit LED in this switch. Actual introduction of the CRC in the generated bit stream takes place only when the SINGLE key (6) is depressed or when the CONT key (10) is lit. When the THRU mode prevails, CRC errors can only be introduced when depressing the SINGLE key (6).
The CRC ERR latent selection can only be made when the system selection is D5-Fe.

3 **FR BIT ERR** -- When this switch is depressed a latent selection is made as indicated by the lit LED in this switch. Actual introduction of framing bit errors in the generated bit stream takes place upon depressing keys 6 through 9 or when the CONT key (10) is lit. When the THRU mode prevails frame bit errors can only be introduced when depressing the SINGLE key (6). The FR BIT ERR selection is mutually exclusive with the CRC ERR or the BPV selection.

4 **BPV** -- When this switch is depressed a latent selection is made as indicated by the lit LED in this switch. Actual introduction of bipolar violations in the generated bit stream takes place upon depressing the SINGLE key (6) or when the CONT key (10) is lit. The BPV selection is mutually exclusive with the CRC ERR and the FR BIT ERR selection.

5 **20 ZEROS** -- A sequence of 20 consecutive zero state bits can be introduced in the bit stream each time this key is depressed while the ALL ONES code is sent continuously.

6 **SINGLE** -- Whenever this key is legitimately depressed the latent selection in this section is activated once. This selection is not legitimate when either the YEL ALARM or the ALL ONES code is being generated.

7 **2/6** -- When this key is legitimately depressed and the system selection is either D1D, D2, or D3/D4/D5, two F_T bits in one sequence of 6 consecutive F_T bits have their state reversed. Alternatively, if the system selection is D5-Fe, framing bits #4 and #24 have their state reversed once. This selection is not legitimate when the THRU mode prevails, when either the YEL ALARM or the ALL ONES code is being generated or when the FR BIT ERR is not selected.

8 **2/5** -- When this key is legitimately depressed and the system selection is either D1D, D2, or D3/D4/D5, two F_T bits in one sequence of 5 consecutive F_T bits have their state reversed. Alternatively, if the system selection is D5-Fe, framing bits #4 and #20 have their state reversed once. This selection is illegitimate when the THRU mode prevails, when either the YEL ALARM or the ALL ONES code is being generated or when the FR BIT ERR is not selected.

9 **2/4** -- When this key is legitimately depressed and the system selection is either D1D, D2 or D3/D4/D5 two F_T bits in one sequence of 4 consecutive F_T bits have their state reversed. Alternatively, if the system selection is D5-Fe, framing bits #4 and #16 have their state reversed once. This selection is not legitimate when the THRU mode prevails, when the YEL ALARM or the ALL ONES code is being generated or when the FR BIT ERR is not selected.

10 **CONT** -- When this key is legitimately depressed, the latent error selection in this section is activated continuously.

As a result, CRC and frame bit errors occur at a rate of one per nine milliseconds or about 110 times per second; BPV's occur at the rate of 5 per second.
This selection is not legitimate when
-THRU mode and CRC ERR are selected
-THRU mode and FR BIT ERR are selected
-YEL ALARM is being generated
-ALL ONES is being generated

Miscellaneous

38 **SELF-TEST FAILURE** -- This LED has three possible states: off, flashing or solidly on. If no operational discrepancy has been detected upon completing the self-diagnostic check the LED is off. If, on the other hand, the digital tone synthesizer experiences a problem the LED flashes on and off. If the front panel microcontroller experiences an operational problem the LED is turned on continuously. The digital tone synthesizer self-testing sequence is initiated each time the frequency or level selection is changed. The front panel micro-controller self-testing sequence is initiated at power up.

39 **PCM OUTPUT FORMAT** -- This key selects alternatively with each depression either AMI (alternate mark inversion) or the B8ZS format as identified by the corresponding LED. When the 515A operates in the THRU mode, the FORMAT selection is under the control of the T-COM 220A or 320A.

40 **PCM OUTPUT MON** -- This jack provides access to the T1 PCM output (40) via two resistors of 430 ohms in the same manner as a monitor jack in the DSX bay.

41 **PCM OUTPUT T1** -- This jack (41) provides access to the PCM bit stream generated by the 515A.

42 **POWER ON/OFF** -- This switch controls the powering of the 515A.

3.3 REAR PANEL FEATURES

The 515A rear panel features are described below. The description numbers match the numbers on figure 3.2.

1 **DSO DATA INPUT** -- This jack is installed as part of option 515A-01 only. This input is compatible with the logic mode.

2 **DSO TIMING SOURCE** -- This 5 position male connector is installed as part of option 515A-01 only. It provides both the 8 kHz and the 64 kHz clocks in a balanced format.

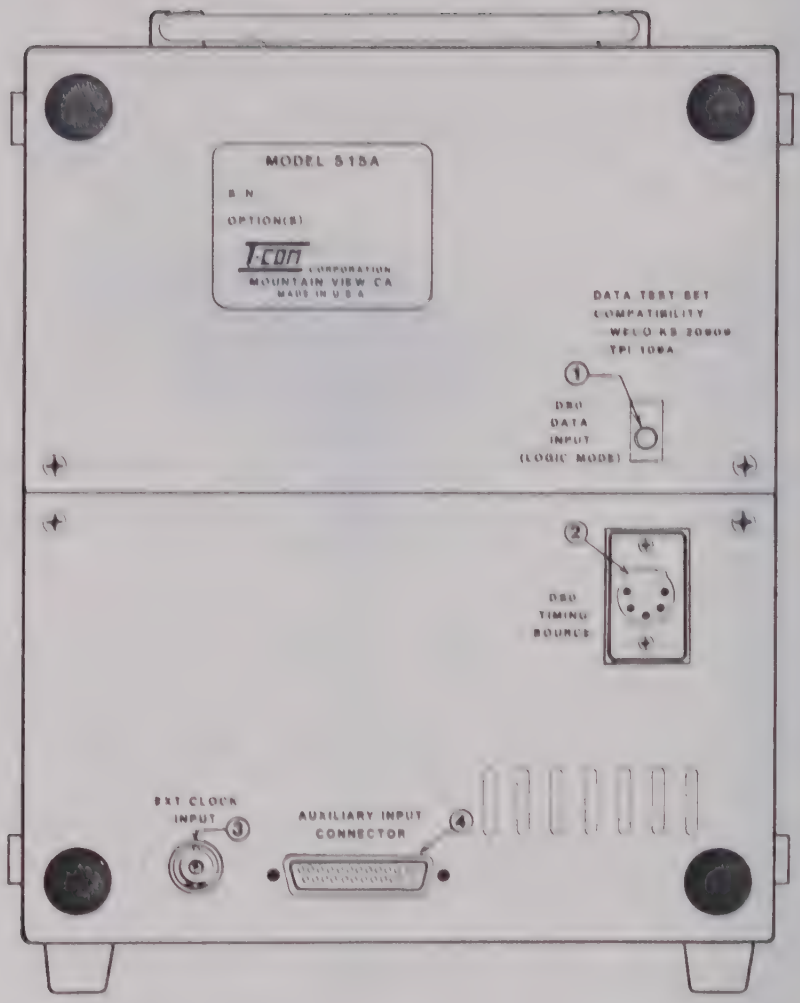


Figure 3.2 Rear Panel Features

3 **EXTERNAL CLOCK INPUT** -- When the 515A is not used in the THRU mode, the PCM clock rate can be controlled by an externally provided clock presented to this BNC connector. Clock source selection is performed automatically by the 515A when it senses the presence of the externally applied clock.

4 **AUXILIARY INPUT CONNECTOR** -- This 25 position D-sub female connector provides access to the data link messages and other timing inputs required for the drop-and-insert mode.

3.4 SIDE PANEL FEATURES

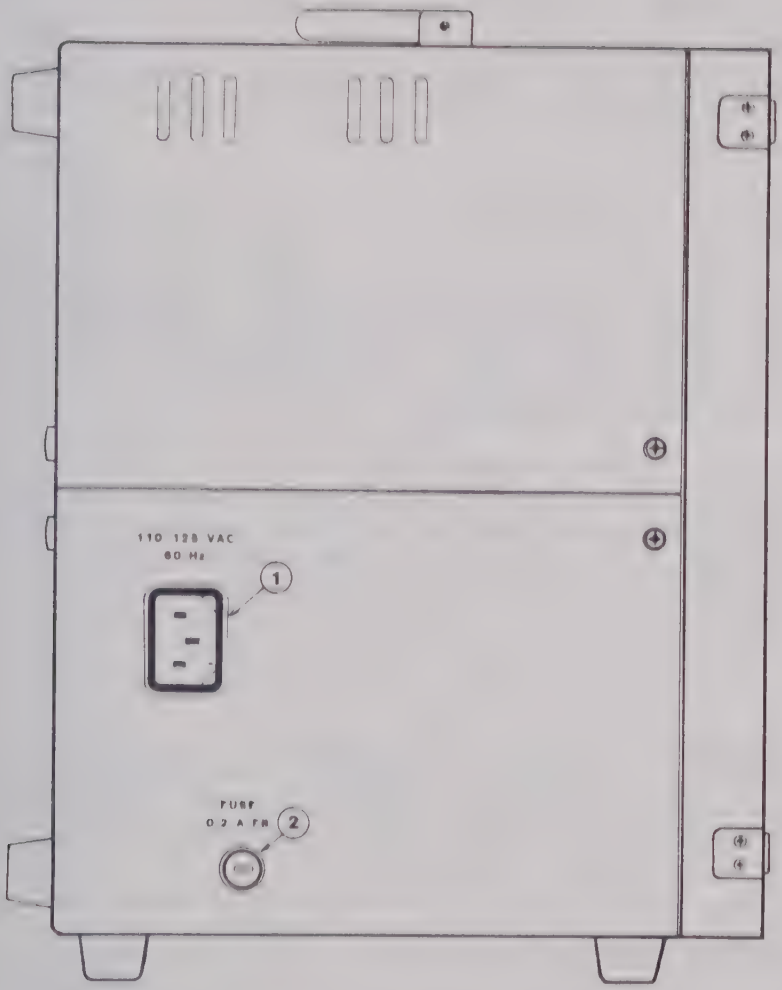


Figure 3.3 Side Panel Features

1 110/125 VAC -- This three-prong inlet connects the supplied AC power cord to a commercial AC source.

2 FUSE -- .20 A fast blow.

3.5 OPERATIONAL CAPABILITIES

The model 515A offers a broad range of PCM bit stream generation capabilities. It can be used either in a stand-alone simulator mode or, when operated in combination with the T-COM 220A or the 320A, to provide DS1 drop-and-insert capability.
To facilitate the description of the 515A PCM simulation capabilities, framed and non-framed PCM generation modes are covered separately below.

3.5.1 Capability Selection

The selection of the capabilities described in the following paragraphs is made either by depression of specific keys, by the insertion of plugs into jacks or by the electrical selection on a connector. In all cases the selection is identified by a dedicated LED on the front panel.

Although the set includes many mutually exclusive features, the use of the 515A is greatly facilitated by the audible and message feedback associated with the keying-in process. A single audible beep accompanies each legitimate key entry. When, on the other hand, an illegal key entry is attempted, a set of two beeps (no...no!) results and in most cases an LED associated with the proximate cause of rejection flashes briefly. When a key entry is rejected, no change to the current status results.

To enhance readability in the capability descriptions which follow, references to specific keying sequences are avoided. While in most cases the keying selection is intuitively obvious, when in doubt, please refer to the detailed feature descriptions in paragraphs 3.2 through 3.4 above.

3.5.2 Framed PCM Generation

A framed DS1 bit stream can be generated by the 515A when it is operated in either the stand-alone simulator mode or the drop-and-insert mode. DS1 framing compatibility includes both normal and extended framing format.

Framed PCM bit streams generated by the 515A are channelized and yield 24 channels each with a capacity of 64 kb/s and one channel with a capacity of 8 kb/s to carry overhead and/or framing data. The content of the 24 channels can be selected as follows:

- one channel can carry any one of the following signal combinations:
  a) an externally supplied 64 kb/s DS0 data signal (with Option 515A-01 only)

b) an internally generated digital tone along with out-of-band signaling either internally selected or externally supplied
c) an externally supplied VF signal along with out-of-band signaling either internally selected or externally supplied

- in the stand alone simulator mode, the other 23 channels may identically contain either the idle code (11111111) or a synthesized digital tone of 1005 Hz at -20 dBm0. In both cases the out-of-band signaling corresponds to the busy state.
- in the drop-and-insert (or THRU) mode the content of the other 23 channels is identical to that monitored by the T-COM 220A (or 320A) on line 1.

The wide range of test signals available in the selected channel makes it possible to simulate the conditions necessary to evaluate most transmission parameters associated with the system receive half-channel. Set-ups required to perform these measurements are given in section 3.6.

When generating framed PCM, the 515A provides for the introduction of messages as well as of impairments in the delivered bit stream. This allows for the testing and evaluation of transmission performance under non-ideal conditions.

3.5.2.1 Framed PCM Messages

Two types of messages can be introduced in the framed PCM bit stream when the 515A is operated in the stand-alone simulator mode only:

- the yellow alarm can be called for various selectable durations
- when the D5-Fe system format is selected, the 4 kb/s data link can be accessed to carry externally provided data. (This data link is a part of the 8 kb/s channel described in paragraph 3.5.2.)

When operating in the framing format compatible with D1D, D2, D3 or D4 banks, the yellow alarm is sent by setting the second most significant bit in each channel to state 0. In this case, the message can be sent continuously or for a duration of either 30 or 50 milliseconds.

When operating in the D5-Fe framing format the 4 kb/s data link is preempted by the yellow alarm code pattern. This pattern can be generated in a continuous manner or for either 13 or 18 times. (The data link carries an all-ones code when idle.)
Access to the data link is provided via the 25 position rear panel mounted connector. Details for this access/interface are given in section 5 of this manual.

3.5.2.2 Framed PCM Impairments

Three types of impairments can be introduced in the framed PCM bit stream. When the 515A is operated in the drop-and-insert mode the impairment injection rate is severely limited to avoid causing a "crash" of the system under test.

When operating in the D5-Fe mode only, CRC errors can be introduced as a single event; in the stand-alone simulator mode it is also possible to introduce CRC errors at the rate of 110/second. (A CRC, or cyclic redundancy check error, means that at least one logic error occurred in the previous 24 frames.)

Terminal framing bit errors can be introduced as a single event; in the stand-alone mode it is also possible to introduce a set of two terminal framing bit errors in a group of 6, 5 or 4 consecutive terminal framing bits or to introduce terminal framing bit errors at a rate of 110/second.

Bipolar violations can be introduced either as a single event or at a rate of 5/second in both the stand-alone simulator mode or in the drop-and-insert mode.

The introduction of impairments is mutually exclusive with the yellow alarm messaging.

3.5.3 Non-Framed PCM Generation

Non-framed PCM bit streams can be generated only when the 515A is operated in the stand-alone mode. Because non-framed PCM is inconsistent with channelization, when a non-framed bit stream is generated the channel selection is disabled as indicated by the lit LED 13 in figure 3.1 and all LED's in the OTHER CHANNELS section are off.

Three types of non-framed PCM bit streams can be generated by the 515A: the all-ones code, the loop-up code and the loop-down code.

The all-ones code can be delivered either continuously or for a duration of 30 or 50 milliseconds. When the all-ones code is generated in a continuous manner, a sequence of 20 consecutive zero state bits can be inserted in the bit stream on a single event basis.

The loop-up code is delivered for 5 seconds following the selection. This code consists of a repeating sequence of 10000; it is required by a remotely located customer service unit (CSU) to provide loop-back

The loop-down code is delivered for 5 seconds following the selection. This code consists of a repeating sequence of 110; it

is required by the CSU to re-establish the normal transmission path.

3.5.4 External PCM Clock Rate Control

When operating in the stand-alone simulator mode the clock rate of the PCM generated by the 515A is normally derived internally from a crystal controlled oscillator. If desired, it is possible to control the generated PCM clock rate by applying an external clock signal meeting the requirements outlined in paragraph 5.4. This is useful if it is necessary to simulate a jittered PCM bit stream or to offset the PCM clock rate from its nominal value.

When operating in the drop-and-insert mode the clock rate of the PCM generated by the 515A is controlled by the clock recovered from the bit stream monitored by the T-COM 220A or 320A on line 1. In this mode, a clock presented to the rear panel BNC connector is superseded by the clock supplied by the monitoring instrument.

3.5.5 DSO Data Test Set Interface (Option 515A-01)

This option provides for the electrical interface with the data test sets made respectively by WECO as the model KS 20909 and by Tele-Path Industries as the model TPI 109A. These instruments provide a family of data patterns suitable for testing the data transmission integrity of various data dedicated channel units. The interface includes both timing and data access.

Detailed information on this interface is provided in section 5.

3.5.6 Digital Tone Synthesizer

This crystal controlled synthesizer provides a highly repeatable and accurate source of tones selectable by steps of 10 Hz over the frequency range of 10 Hz to 3990 Hz and by steps of 0.1 dB over the level range of +3.2 to -59.9 dBm0.

It should be noted that an error of approximately +0.4% has been introduced by design in the tone frequency. This ensures that none of the generated tones is a subharmonic of the 8000 Hz system sampling frequency and thus avoids the possibility of undesirable beating. As a result of this error, however, the actual frequency is, for example, 1004 Hz when the level selection reads 1000 Hz.

When the frequency or the level settings are out of range the synthesizer delivers the idle code (11111111).

3.5.7 PCM Output

Regardless of framing, the PCM output can be formatted for compatibility with either AMI (alternate mark inversion) or B8ZS (bipolar with 8 zeros substitution) systems. When operated in the drop-and-insert mode this selection is made automatically by the controlling T-COM 220A or 320A in response to the format monitored by either instrument.

The PCM OUTPUT T1 can be used to drive any 100 ohm line or circuit; it is balanced and insulated from the chassis ground. The PCM OUTPUT MON can be used as any monitor jack at the DSX-1 bay.

3.6 OPERATING INFORMATION

This section provides application related information to facilitate the use of the 515A for its intended purposes.

This section covers:

- preparation for operation
- stand-alone PCM simulator operating mode
- drop-and-insert operating mode

3.6.1 Preparation for Operation

The instrument is turned on by setting the toggle switch 42 in figure 3.1 to ON.

Upon power-up the front panel microcontroller and digital tone synthesizer processor execute a comprehensive self-check procedure to ensure operational integrity. If both processors determine no evidence of operational fault all front panel LED's are turned on for a few seconds, allowing the user to determine that none is burned out. The bicolor LED's associated with the internal signaling state selection alternatively flash the red and green colors. At the end of the cycle all LED's are turned off except for those indicating the default status.

If an operational error is identified by the front panel microcontroller, the SELF-TEST FAILURE LED is held solidly on at the end of the LED test. If the synthesizer identifies a failure, the SELF-TEST FAILURE LED flashes on and off.

Two distinct default modes are provided to accommodate the stand-alone simulator mode and the drop-and-insert mode, respectively.

- Stand-alone simulator mode default settings when no external connections to the set are made and a legitimate channel number is selected:

- SYSTEM	:	D3/D4/D5
- IMPAIRMENTS	:	BPV
- SELECTED CHANNEL	:	INT TONES/CODES INT SIGNALING A and B red on
- OTHER CHANNELS	:	IDLE
- MESSAGES	:	YEL ALARM
- PCM OUTPUT FORMAT	:	AMI

- Drop-and-insert mode default settings: (the 515A is connected to a T-COM 220A or 320A via the 25 position rear panel connector and the PCM monitoring set is powered-up)

- SYSTEM	:	as selected by the PCM monitoring set
- IMPAIRMENTS	:	BPV
- SELECTED CHANNEL	:	DIS'D LED lit, other settings in this section depend on external connections
- OTHER CHANNELS	:	THRU
- MESSAGES	:	YEL ALARM
- PCM OUTPUT FORMAT	:	as selected by the PCM monitoring set

Note: in the event of a self-test failure, it is recommended to turn the power off and to restore it a moment later. This can sometimes clear a spurious problem.

3.6.2 Stand-Alone PCM Simulator Operating Mode

Figure 3.4 shows the basic operating configuration. In this mode the 515A provides a family of stimuli needed to perform a variety of transmission tests on equipment in an out-of-service condition. Basically three types of testing are made possible in this configuration:

1 - testing with non-framed PCM signals
2 - testing PCM framing and other related system capabilities
3 - performing half-channel transmission performance characterization

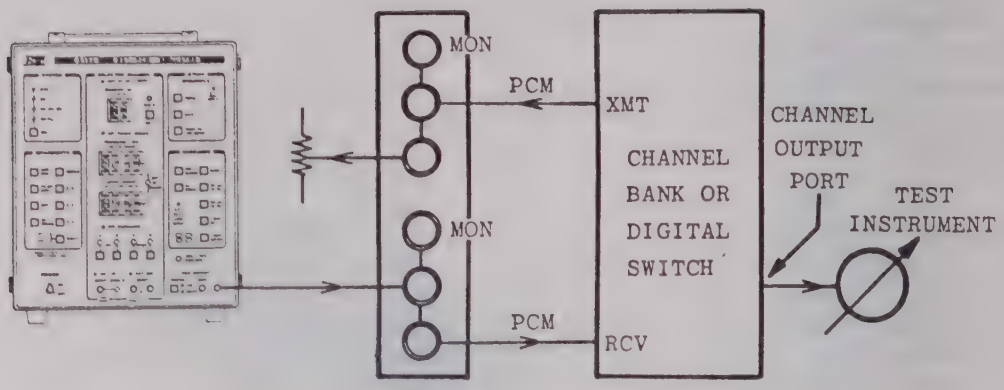


Fig. 3.4 Stand-Alone Mode Basic Operating Configuration

3.6.2.1 Applications using unframed signals include:

- keeping a PCM line alive using the all-ones signal
- evaluating the response time of an all-ones code detector
- evaluating the ability of a carrier detector to recognize the loss of PCM by introducing 20 consecutive zeros in the all-ones code
- setting a remote CSU in the loop mode
- resetting a CSU to the normal transmission mode

To perform the desired test it is simply required to connect the 515A T1 PCM output to the equipment or system under test and to set the conditions on the simulator front panel as required.

3.6.2.2 Applications using framed signals include:

- evaluating the robustness of the framing circuitry under test by subjecting it to various rates of framing bit errors
- evaluating the effectiveness of CRC error detecting circuitry in systems using the extended framing format
- determining the detection threshold of the yellow alarm code in systems using either the D3 or the extended framing format
- testing the ability to detect bipolar violations
- testing the ability to recognize B8ZS formatted PCM
- testing the messaging capability of the data link associated with the extended framing format
- evaluating the performance of a transmission system in the presence of calibrated clock jitter, obtained by supplying a jittered clock externally to the 515A

To perform any of the tests outlined above it is simply required to connect the 515A T1 PCM output to the equipment or system under test and to set the conditions on the simulator front panel as required. Introduction of an externally supplied message in the data link requires the interfacing of the message source with the 25 position rear panel mounted connector. For details on this interface, refer to section 5 of the manual.

3.6.2.3 Half Channel Transmission Performance Testing

When the 515A is used in combination with other test instruments, it is possible to perform a variety of transmission tests to characterize the transmission performance of the decoder/receive half of a channel independently of the encoder half.
General test set-ups and procedures are provided below to facilitate the evaluation of the following parameters:

Parameter	Chart No.	Fig.
Gain	3-A	3.5
Gain linearity	3-B	3.5
Frequency response	3-C	3.5
Cross-talk	3-D	3.5
Idle noise	3-E	3.5
In-band signaling	3-F	3.6
E & M signaling	3-G	3.7
Data integrity	3-H	3.8

Chart 3-A Receive Half-Channel Gain Measurement

Step	Procedure
1	Set the 515A controls as follows: - System selection to match the type of channel bank under test - Channel selection to correspond to the channel number under test - Internal tone frequency : 1000 Hz - Internal tone level : 0.0 dBm0 - Other channels : IDLE - Messages : No active selection - Impairments : No active selection - PCM output format : as required
2	Set the level and noise meter controls as follows: - Input impedance to match the channel unit output impedance - Level measurement selection
3	Obtain the receive gain by direct reading of the level on the level meter

Chart 3-B Receive Half-Channel Gain Linearity Measurement

Step	Procedure
1	Set the controls on the 515A and the level and noise meter as described in Chart 3-A steps 1 and 2
2	Set the 515A internal Tones/Codes level selection successively to the set of desired level points in the range of +3.2 to -59.9 dBm0.
3	For each setting of step 2 obtain the corresponding level reading on the level and the noise meter
4	Obtain the gain linearity error by taking the difference between the level set on the 515A and the level read on the level and noise meter

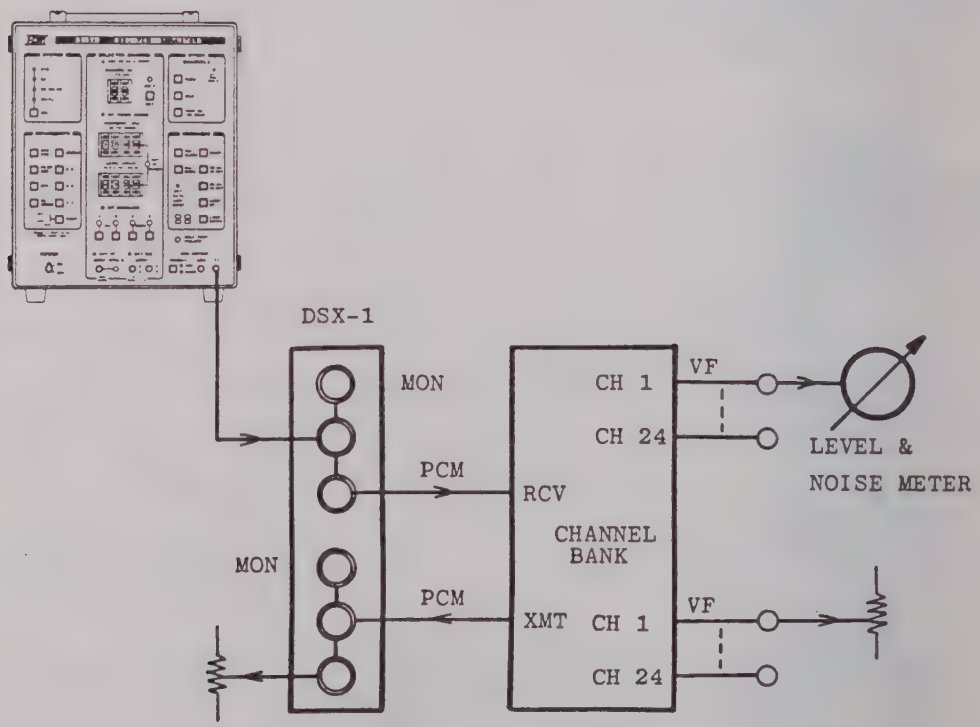


Fig. 3.5 Receive Half Channel Gain Linearity Measurement

Chart 3-C Receive Half-Channel Frequency Response Measurement

Step	Procedure
1	Set the controls on the 515A and the level and noise meter as described in Chart 3-A steps 1 and 2
2	Set the 515A internal Tones/Codes frequency selection successively to the set of desired frequency points in the range of 200 Hz to 3990 Hz
3	For each setting of step 2 obtain the corresponding level reading on the level and noise meter
4	The plot of each level reading against the set frequency yields the frequency response.

Chart 3-D Receive Half-Channel Cross-Talk Measurement

Step	Procedure
1	Set the controls on the 515A and the level and noise meter as described in chart 3-A steps 1 and 2
2	Terminate the receive port of the channel unit under test to its nominal impedance using a discrete resistor
3	Connect the level and noise meter to the channel unit for which the cross-talk measurement is required
4	The direct reading of the level on the level and noise meter yields the cross-talk attenuation

Note: greater accuracy of the cross-talk measurement can be obtained by substituting a selective level meter for the level and noise meter. In this case the selective level meter frequency setting must be 1004 Hz.

Chart 3-E Receive Half-Channel Idle Noise Transmit

Step	Procedure
1	Set the controls on the 515A and the level and noise meter as described in Chart 3-A steps 1 and 2
2	Set the 515A Channel No. to 00 and observe that the DIS'D LED is lit
3	Set the level and noise meter to C-message weighting
4	The direct reading of the noise meter yields the idle noise measurement for the channel monitored by the noise meter

Chart 3-F Receive Half-Channel In-Band Signaling Measurement

Step	Procedure
1	Set the 515A controls as follows: - System selection to match the type of channel bank under test - Channel selection to correspond to the channel number under test - External VF : active - Internal Signaling : any state - Other Channels : IDLE - Messages : no active selection - Impairments : no active selection - PCM output format : as required
2	Set the in-band signaling test set No. 1 controls to deliver the sequence of tones associated with a dialed sequence of digits. Select the mode (DTMF, MF, SF) and tone level as required by the channel unit under test
3	Set the in-band signaling test set No. 2 controls to receive the type of signaling generated by the sending set
4	Verify signaling integrity by comparing the signaling messages delivered by the sender test set with the signaling messages received by set No. 2

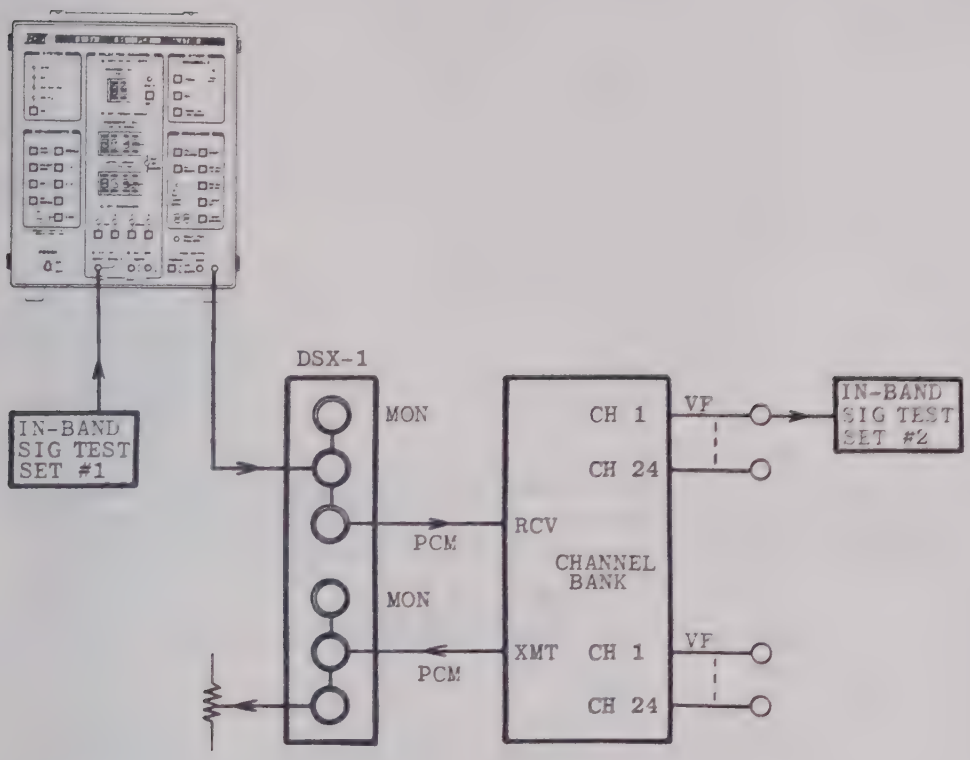


Fig. 3.6 Receive Half-Channel In-Band Signaling Measurement

Chart 3-G Receive Half-Channel E & M Signaling Measurement

Step	Procedure
1	Set the 515A controls as follows: - System selection to match the type of channel bank under test - Channel selection to correspond to the channel number under test - Internal Tones/Codes : 1000 Hz - External Signaling : active - Other Channels : IDLE - Messages : no active selection - Impairments : no active selection - PCM output format : as required
2	Set the E & M signaling test set No. 1 controls to deliver the sequence of pulses associated with a dialed sequence of digits. Select the pulse make/break ratio and frequency as required
3	Set the E & M signaling test set No. 2 controls to receive the pulse sequence delivered by the sending set
4	Verify signaling integrity by comparing the signaling messages delivered by the sender test set with the signaling messages received by set No. 2.

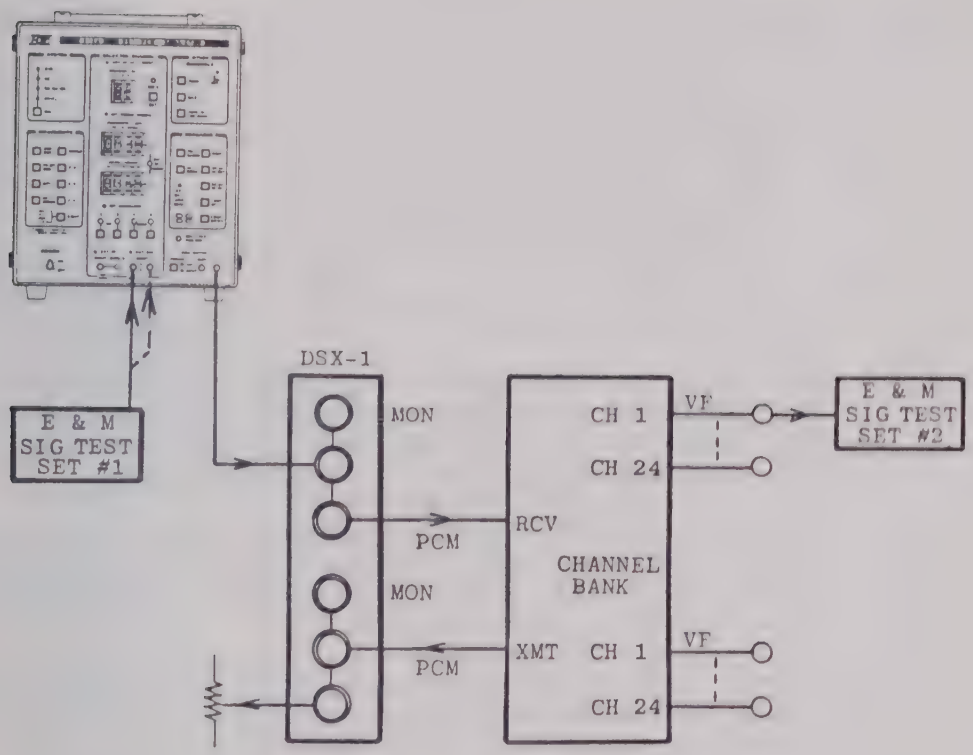


Fig. 3.7 Receive Half-Channel E & M Signaling Measurement

Chart 3-H Receive Half-Channel Data Performance Testing

Step	Procedure
1	Set the 515A controls as follows: - System selection to match the type of channel bank under test - Channel selection to correspond to the channel number under test - Auxiliary 64 kb/s input : active - Other Channels : IDLE - Messages : no active selection - Impairments : no active selection - PCM output format : as required
2	Set the KS 20909 data test set controls to deliver the desired data sequence according to the type of data channel unit under test. Data must be presented to the 515A in the logic mode
3	Set the KS 20908 data test set controls to receive the pulse data sequence delivered by the sending set. Data delivered by the 220A on the DSO output is in the logic mode
4	Verify the data decoding integrity by comparing the data delivered by the KS 20909 with the data received by the KS 20908 test set

Note: data transmission errors can be readily detected by setting the two data test sets in the quasi-random word generation/detection mode: i.e. 511 or 1047. In this mode the KS 20908 bit error counter accumulates the detected bit errors during the test

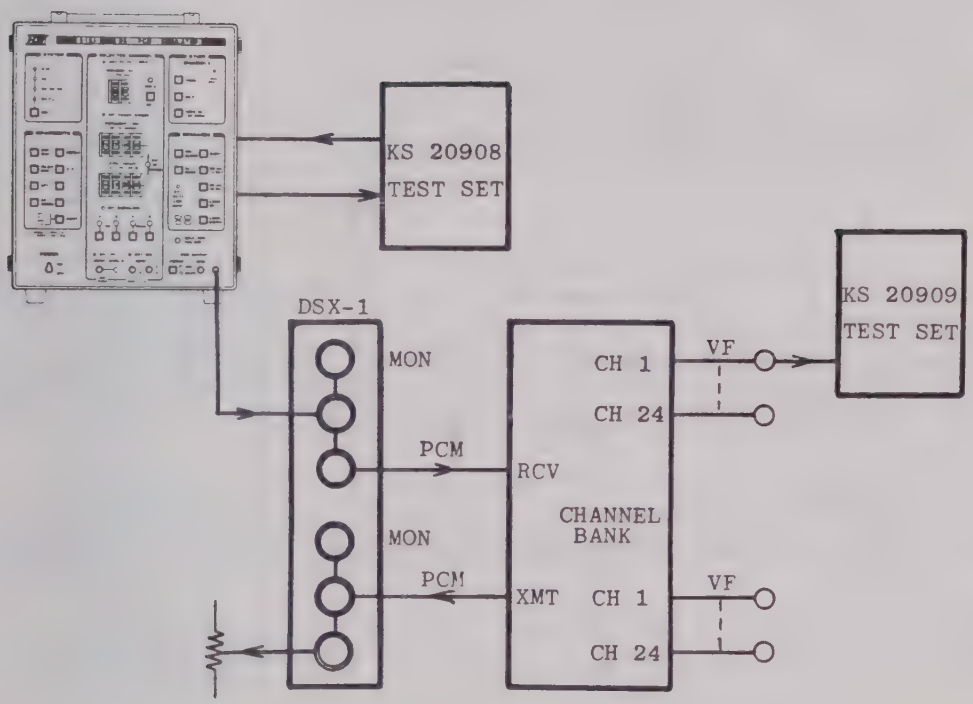


Figure 3.8 Receive Half-Channel Data Performance Testing

3.6.3 Drop-and-Insert Operating Mode

Figure 3.9 shows the basic operating configuration. In this mode the 515A provides primarily the means of performing tests on one channel without affecting the traffic in the other 23 channels. The receive half-channel transmission parameters associated with VF, data and signaling can be characterized as outlined in paragraph 3.6.2.3. A limited amount of PCM impairments can also be introduced in the outgoing bit stream.

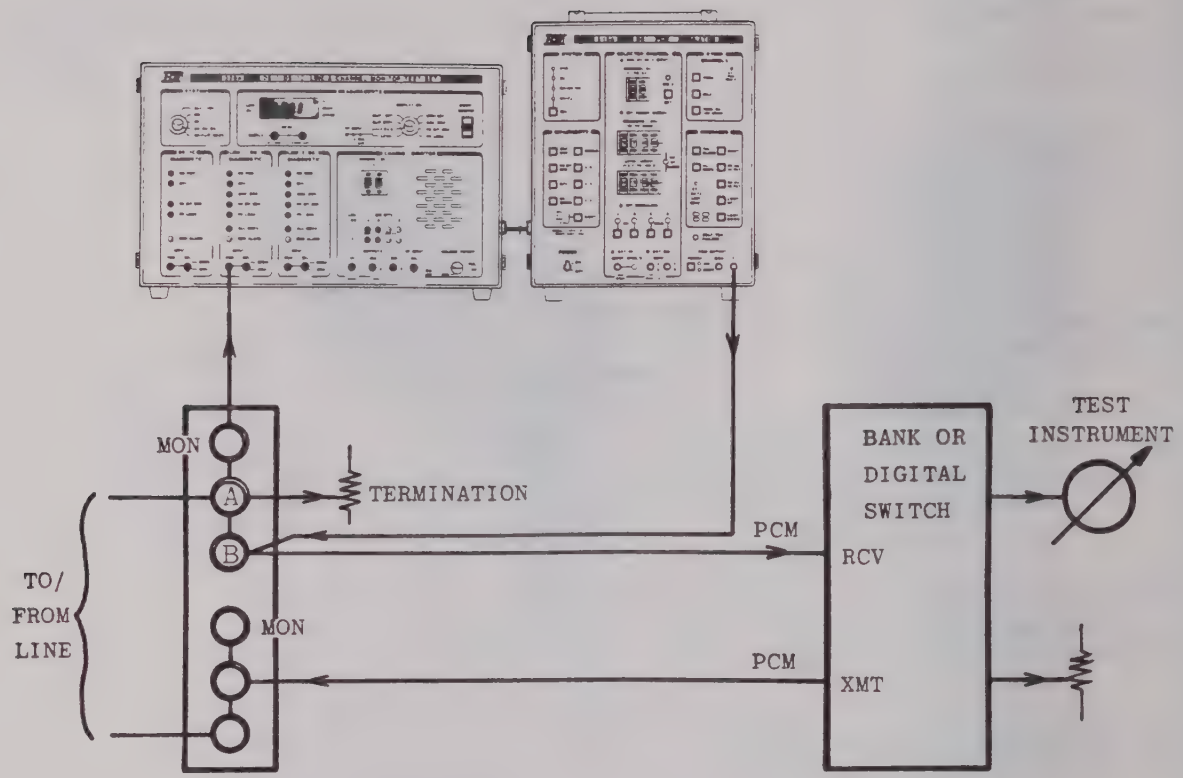


Fig. 3.9 Drop-and-Insert Mode Basic Operating Configuration

To set up the drop-and-insert mode one must carry-out the following steps:

- connect the T-COM 220A (or 320A) 25 position connector to a similar connector on the 515A rear panel using the T-COM cable number 2070-014
- power-up both instruments and reset the 220A
- set the 220A controls as follows:
  - SYSTEM selection : according to the system under test
  - CHANNEL SEL : as desired
  - VF INPUT : 1
  - MEASUREMENT controls : as desired
  - LINE 1 PCM INPUT SEL : MON
- connect a patch cord between the DSX-1 bay monitor jack and the 220A LINE 1 PCM INPUT
- observe that all the LED's in LINE 1 DIAGNOSTIC section are off and that LINE 1 signaling LED's in the CHANNEL MONITOR section are lit
- depress the THRU key on the 515A and observe that:
  - the system selection and the PCM format selection are identical on the 220A and the 515A

- the 515A channel selection is disabled
- connect the 515A T1 PCM output to the DSX-1 jack B in figure 3.5 and, at the same time, plug a 100 ohm termination into jack A. System transmission disruption is minimized by acting swiftly when inserting these two plugs.

At this point the 220A/515A combination acts as a transparent connection to the transmission. The 220A's full range of monitoring capabilities can be exercised without introducing any interference in the traffic. When ready to insert a signal into a channel proceed as follows:

- ensure that the channel to be tested is idle
- select the channel content as desired
- depress the SET key (number 14 in figure 3.1) to enable the selection. If the number for the selected channel is legitimate the DIS'D LED turns off upon depressing the SET key

At this point 23 out of 24 channels are transparently connected through the 220A/515A combination and the channel selected by the 515A is pre-empted and contains the signals selected in the 515A SELECTED CHANNEL section.

To introduce the least amount of disruption in the transmission when exiting the drop-and-insert mode, swiftly and simultaneously remove the plugs from jacks A and B in the DSX-1 bay.

Note: Although the use of the terminating resistor is highly recommended to maintain optimal signal shape and level at the monitor jack when the line is opened, in some cases the 220A can operate satisfactorily when this termination is not provided. The determining factor is the amount of pulse distortion present at the monitored point.

4. TECHNICAL DESCRIPTION

4.1 INTRODUCTION

This section provides a general description of the model 515A architecture and operation at the block diagram level.

4.2 ARCHITECTURE

The 515A is partitioned into 5 main sections. These sections happen to correspond to physical assemblies; they are interconnected as shown in figure 4.1 These assemblies are:

1. the front panel circuit board
2. the digital tone synthesizer
3. the simulator circuit board
4. the DSO interface (option 515A-01), and
5. the power supply/mother board assembly

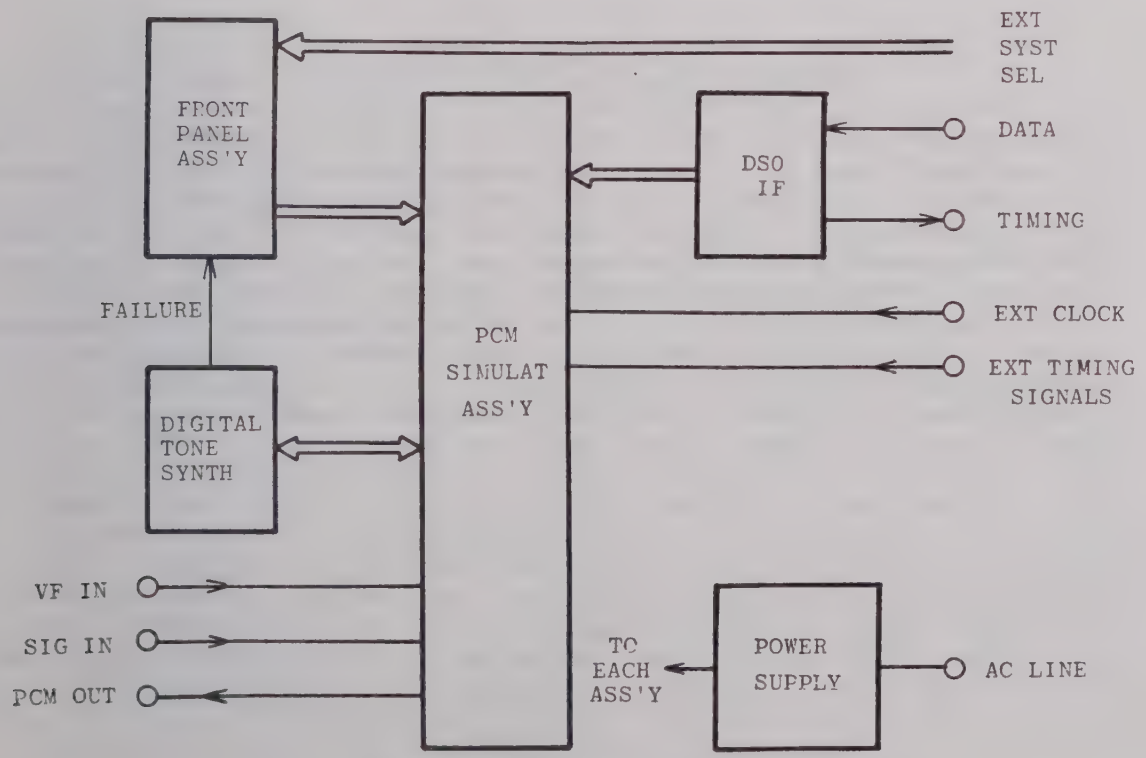


Fig. 4.1 General Block Diagram

The front panel assembly basically provides the interface between the human operator and the circuitry performing the actual PCM signal generation function.

The digital tone synthesizer assembly is dedicated to the generation of digital codes corresponding to a wide range of tone level and frequency combinations. The digital signal generated by this assembly is delivered to the simulator circuitry. Like the front panel assembly, the tone synthesizer is controlled by a dedicated processor.

The simulator circuit board generates and delivers the PCM signal combinations under the control of the front panel processor. It interfaces also with the optional DSO access unit, and a number of externally supplied signals.

The DSO assembly interfaces the externally supplied 64 kb/s data stream with the simulator circuit and thus, makes it possible for the simulator to insert this data into the selected channel.

The power supply provides the power required by all the other assemblies.

Each circuit board assembly operation is described at the block diagram level in the following paragraphs.

4.3 FRONT PANEL CIRCUIT BLOCK DIAGRAM

A simplified block diagram for the front panel assembly is shown in Figure 4.2. Dedicated I/O expander circuits interface the microcontroller, on a time shared basis, with the front panel switches, the LED's, the externally provided electrical control signals and the PCM simulator assembly. The microcontroller continuously scans the array of switches and dispatches the signals required to light the LED's, control the beeper and the PCM simulator assembly. The microcontroller is programmed to accept and reject specific combinations of key entries and externally supplied signals. The microcontroller is also programmed to carry out comprehensive self-diagnostics at power-up.

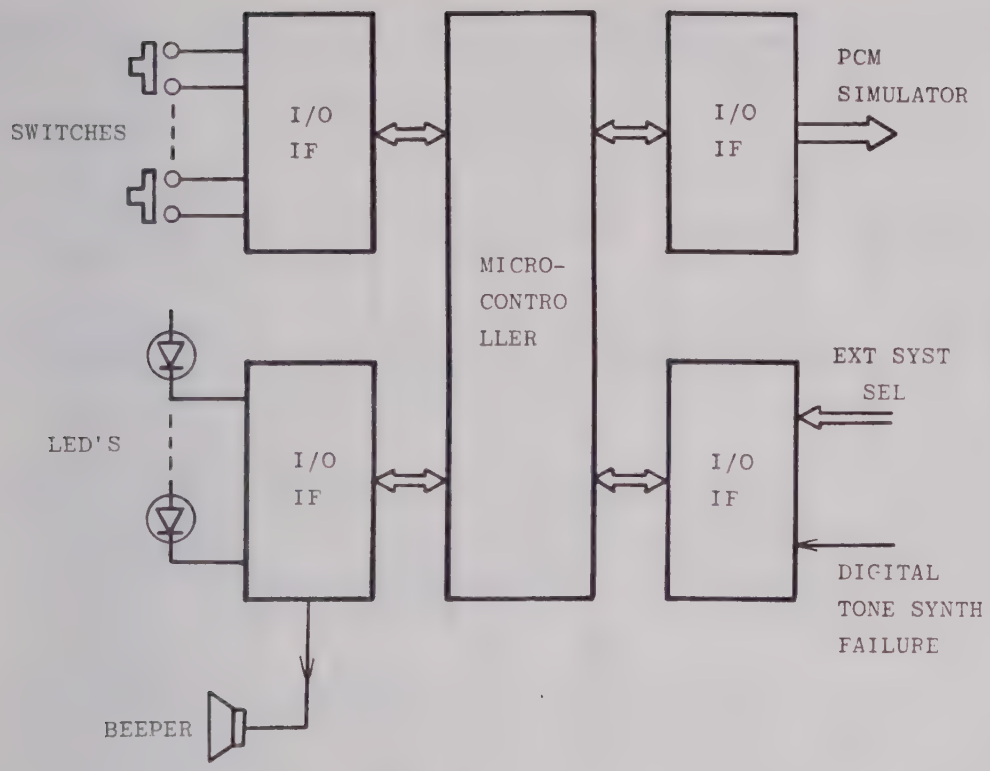


Fig. 4.2 Front Panel Assembly Block Diagram

4.4 DIGITAL TONE SYNTHESIZER CIRCUIT BLOCK DIAGRAM

A simplified block diagram for the tone synthesizer is shown in Figure 4.3. The code switch selection for level and frequency is provided to the microcontroller via a dedicated I/O interface circuit. This interface is periodically scanned by the controller to determine if a change of selection has been made. The microcontroller decodes the selection and determines whether the level and frequency selected are within the acceptable range. If the selection is within the selectable range, the processor synthesizes the family of codes corresponding to the selected combination. If the selection falls outside the acceptable range, the processor generates the idle code (11111111) and provides an output indicating the out-of-range condition. In both cases the microcontroller output data is delivered to an output buffer and the status is delivered to an output interface circuit. The PCM bit stream delivered by the output buffer is synchronized with the bit stream generated by the PCM simulator circuits. When a change in the frequency and/or level selection is made the microcontroller performs a self-diagnostic check. If a failure is detected, the controller asserts a self-test failure

state and stops its operation. This failure state, when received by the front panel processor, causes the flashing of the SELF-TEST FAILURE indicator.

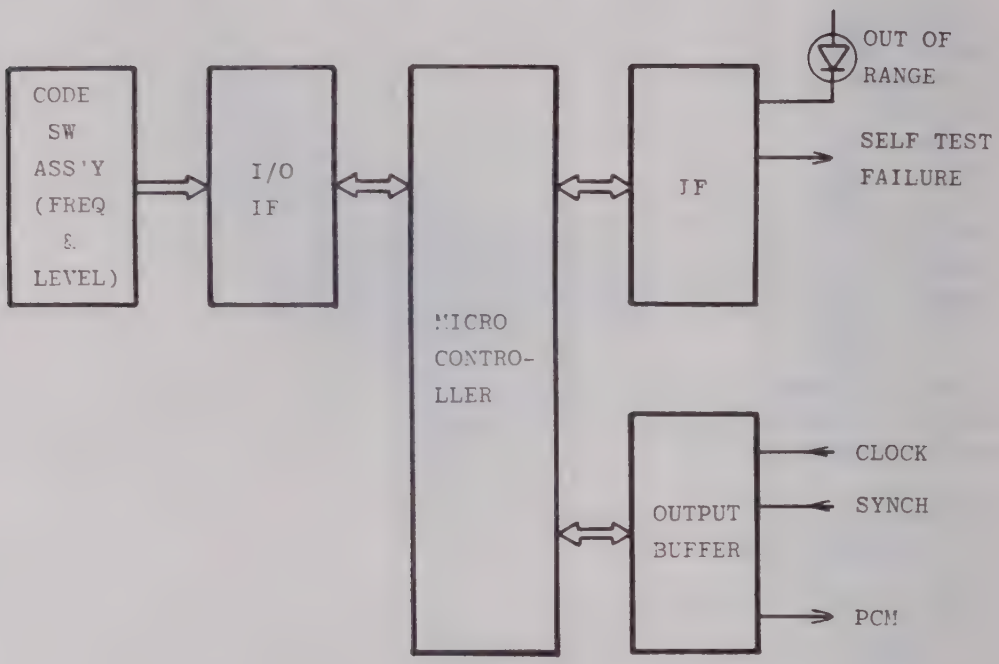


Fig. 4.3 Digital Tone Synthesizer Circuit Block Diagram

4.5 PCM SIMULATOR CIRCUIT BLOCK DIAGRAM

A simplified block diagram for the PCM simulator circuitry is shown in figure 4.4 The lower part of this diagram shows the control leads originating from the front panel assembly. All the other connections terminated by a small circle are associated with other assemblies. To keep the diagram simple the system clock and many secondary timing leads have been omitted.

System clock:
Selector MUX1 can select the system clock from three sources: the internal crystal controlled oscillator, the clock externally supplied to the BNC connector and the clock supplied to the 25 position connector. The selection is controlled by the front panel microcontroller.

Primary PCM signal:
This signal is obtained from the time multiplexing of the signals presented at ports I1 through I6 of multiplexer MUX2. If the THRU mode is selected, the primary PCM signal is identical to the signal delivered by the external PCM source. In the IDLE mode or

the 1005 Hz/-20 dBm0 mode, the primary PCM signal consists of a framed bit sequence of 24 channels all containing the same pattern. When the extended framing format is selected, the signal delivered by MUX2 includes the data link message(s) as well as the CRC code sequence. The data link may be selected to contain either the idle code (an uninterrupted sequence of 1's), an externally supplied 4 kb/s message, or alternatively, the alarm code.

Fe Alarm Code:
This code consists of a sequence of the following 16 bit pattern: 1111111100000000. The alarm code generator can be controlled to deliver a specific number of patterns.

CRC code sequence:
This sequence of 6 bits is obtained from the CRC computer. To generate this code the computer performs a polynomial division of the data contained in the secondary PCM during the previous 24 frame superframe. The CRC generator can introduce errors as required.

Framing bit sequence:
Basically two framing bit sequences can be generated by the frame bit generator: the D3 and the extended framing format. In the D3 format, the framing sequence is 12 bit long. In the extended framing format this sequence is just 6 bit long. In both cases the framing bit generator can introduce framing bit errors as required.

Channel number sequence:
Three different channel sequences can be generated and selected to conform to the D1D, D2, D3/D4/D5 channel numbering sequences, respectively.

Secondary PCM signal:
This signal is obtained from the time multiplexing of the signals presented at ports I1 through I6 of MUX3. This multiplexer basically lets the primary PCM signal on through except during the 8 bit time slot (strobe) associated with the selected channel. During the strobe, the content of the secondary PCM signal can be a combination of encoded tones and signaling or 64 kb/s (DS0) data. When the D3 framing mode prevails and the alarm is raised, MUX3 forces every second most significant bit in every channel to state zero.

Strobe:
This signal is delivered by the magnitude comparator when the channel numbering sequence matches the number selected by the code switches.

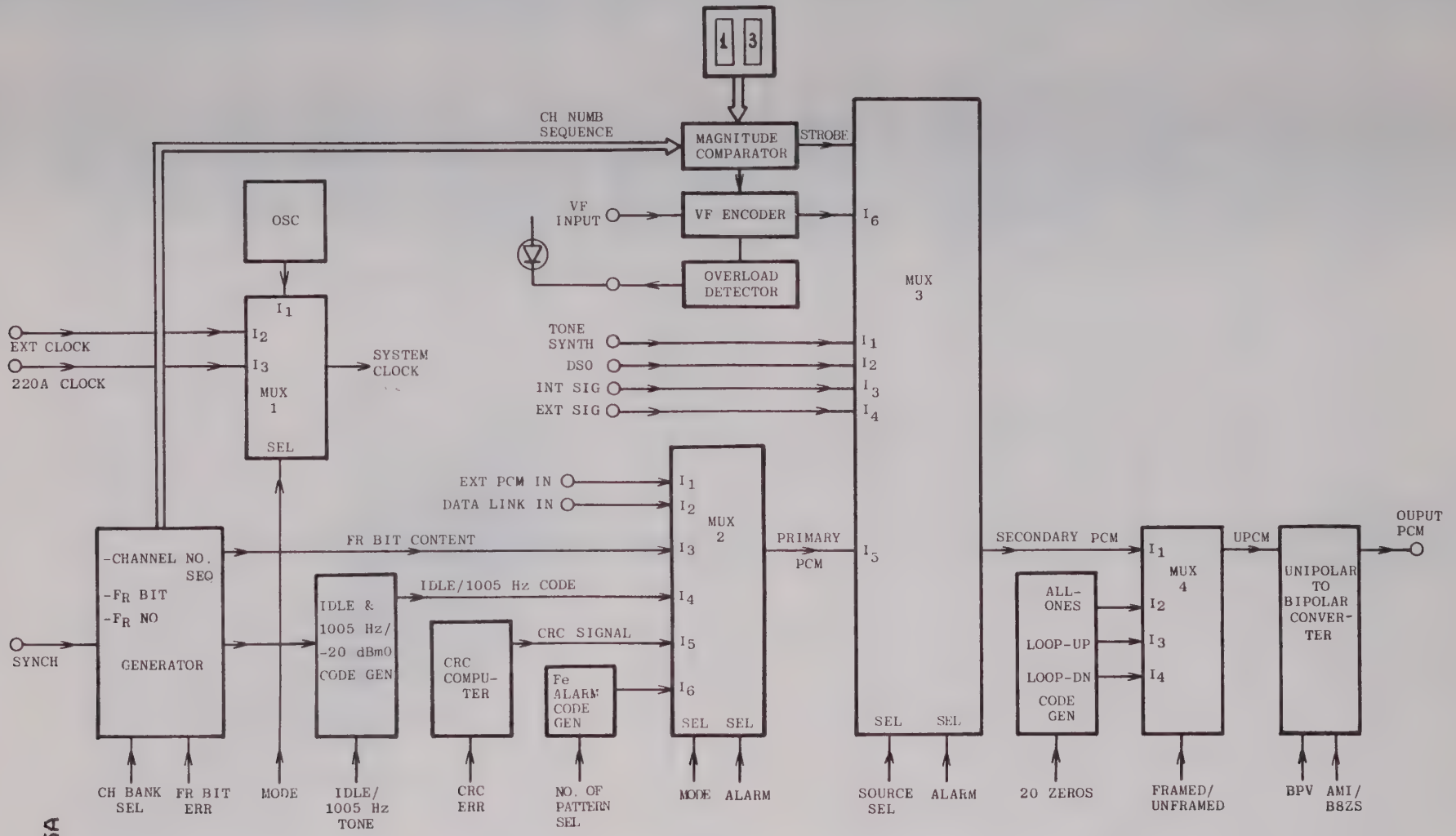


Fig. 4.4 PCM Simulator Circuit Block Diagram

VF encoder:
This circuit basically converts the externally supplied VF signal to a 64 kb/s equivalent bit stream. This encoding process is consistent with the Mu-255 coding law; it is initiated at the onset of the strobe pulse.

UPCM:
This unipolar PCM signal is obtained from the time multiplexing of the signals presented at ports I1 through I4 of MUX4. When a framed format is selected MUX4 lets the secondary PCM on through. When an unframed selection is made instead, UPCM consists of either the all-ones code, the loop-up code or the loop-down code delivered by the code operator. When the all-ones code is selected a sequence of 20 consecutive zeros can be introduced in UPCM.

Unipolar/Bipolar converter:
This circuit primarily converts the UPCM logic signal into a T1 line compatible bipolar format. It can also introduce bipolar violations in the output PCM bit stream as required. Furthermore, when selected to provide B8ZS line format compatibility, this circuit substitutes all sequences of 8 consecutive zero state bits with the B8ZS code.

4.6 DSO ACCESS INTERFACE CIRCUIT BLOCK DIAGRAM

A simplified block diagram for the DSO access interface unit is shown in fig 4.5. This interface provides the timing signals required by the data generator (WECO KS 20909) and accepts the 64 kb/s data stream delivered by this source.

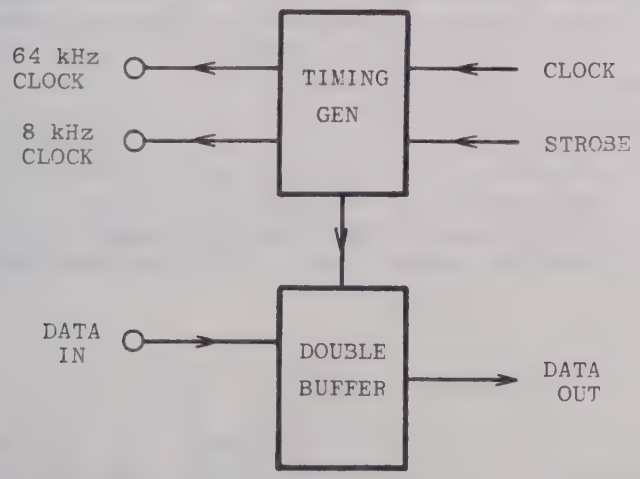


Fig. 4.5 DSO Access Interface Block Diagram

Timing signals:
Both a 64 kHz clock and an 8 kHz clock are generated by the timing generator circuit. This circuit consists primarily of a phase locked oscillator and a divider with multiple outputs. The oscillator delivers a 2.048 MHz clock locked on the 8 kHz strobe signal. The divider, along with some combinatorial logic yield both clocks with the phase relationships shown in fig 5.2. To obtain a balanced drive, both phases of each clock are provided.

Double buffer:
The data supplied by the external source is clocked into the input 8 shift register in synchronism with the 64 kb/s clock. 8000 times per second the content of this buffer is transferred in parallel to a parallel-in, serial-out shift register. The content of this second shift register is downloaded to the simulator circuit during the strobe pulse. In other words, the double buffer takes 125 microseconds to acquire 8 bits of input data and 5.2 microseconds to deliver them to the simulator board.

4.7 POWER SUPPLY CIRCUIT BLOCK DIAGRAM

A simplified block diagram for the power supply circuitry is shown in fig 4.6. The three voltages required by the instrument are obtained by converting the power from the AC line in two successive steps.

AC/DC converter:
This circuit consists primarily of a power transformer, several diodes and large filtering capacitors. The transformer secondary windings delivers 6.3 VAC nominal to the diodes. These diodes are configured as a half-wave rectifier for the -5 V, a full-wave rectifier for the +5 V and a voltage doubler for the +12 V. The large electrolytic capacitors greatly reduce the ripple on the supply voltages.

DC regulator:
This circuit consists, in fact, of three passive regulator devices, each dedicated to a single supply voltage. These regulators yield highly stable power supply voltages with very low noise and ripple over the full operating range of the instrument.

Fig. 4.6 Power Supply Circuit Block Diagram

5. REAR PANEL ACCESS INTERFACE

5.1 INTRODUCTION

This section contains the information necessary for using the input interfaces provided on the 515A rear panel. This information includes a description of the electrical characteristics for each terminal.

5.2 ELECTRICAL INTERFACE DESCRIPTION

The electrical interface found on the rear panel consists of a 25 position female receptacle 'D-Sub' connector, a BNC connector and, if the instrument is equipped with option 515A-01, of a bantam jack and a 5 pin male connector.

The 25 position connector has two purposes: first, it provides a means to input a 4 kb/s data stream to the data link available when the 515A operates in the DS-Fe format; second, this connector is used to input all the signals required to slave the 515A to the T-COM 220A or 320A when implementing the DS-1 drop-and-insert mode.

The BNC connector accepts an external clock to control the rate of the PCM bit stream delivered by the simulator.

The bantam jack accepts the 64 kb/s data stream delivered by a data test set for insertion into the selected channel.

The five pin connector provides the timing signals required by the 64 kb/s data source to deliver a data stream synchronized and appropriately phased with the PCM bit stream generated by the 515A.

Detailed description for each of these connectors is found in tables 5.1 through 5.4 on the following pages.

Table 5.1 25 Position Connector Pin Assignment

Pin No.	Identifier	Description
1	B8ZS*	Low state selects the B8ZS format
2	PCMIN	External PCM signal input
3	GND	Ground
4	RCK	External clock input
5	D1D*	Low state selects the D1D format
6	SYNCH*	System synchronization pulse input
7	-	Key
8	-	N/A
9	-	N/A
10	-	N/A
11	D5-Fe*	Low state selects D5-Fe format
12	-	N/A
13	D3/D4*	Low state selects D3/D4/D5 format
14	GND	Ground
15	EXTDLI	External input to the 4 kb/s data link
16	EXTDLS*	Low state selects the external 4 kb/s data
17	DLCK	4 kHz clock for data link (output)
18	D2*	Low state selects the D2 format
19	-	N/A
20	FAULT*	Low state to declare a fault condition
21	-	N/A
22	-	N/A
23	-	N/A
24	-	N/A
25	ID	+5 V to identify 220A/320A connection

Table 5.2 BNC Connector Terminal Assignment

Terminal	Identifier	Description
Center	Clock	Input for 1.544 MHz nominal
Outer	GND	Ground/clock return

Table 5.3 Bantam Jack Terminal Assignment

Terminal	Identifier	Description
Tip	Data	64 kb/s data input
Ring		open
Sleeve	GND	Ground/signal return

Table 5.4 Five Position Connector Pin Assignment

Pin No.	Identifier	Description
1	GND	Ground
2	8KCLK	8 kHz clock
3	8KCLK	8 kHz clock complement
4	64KCLK	64 kHz clock
5	64KCLK	64 kHz clock complement

5.3 APPLICATION INFORMATION

The signals supplied to the 515A on the rear panel connectors must comply in level, rate and timing relationship with the requirements outlined in section 5.4 to obtain the desired results. The T-COM models 220A and 320A deliver all the signals required to implement the DS1 drop-and-insert operating mode.

The use of the recommended interconnecting cable (T-COM P/N 2700-014) precludes accessing the D5-Fe data link when the drop-and-insert mode is required. This prevents the undesirable disruption of the data link transmission in this mode.

When the 515A is operated in the stand-alone simulator mode and delivers a D5-Fe formatted bit stream, the 4 kb/s data link can carry an externally supplied data stream. This external message must be synchronized to the 4 kHz clock supplied by the 515A on the 25 position connector. To access the data link terminal 16 must be grounded.

The DSO input is compatible with either data polarity by means of a strapping option provided on the DSO assembly. The polarity is set at the factory for non-inversion. When data polarity inversion is desired, the jumper M1 located near U2 and U3 on the DSO interface board must be pulled out and installed in the I (invert) position.

When connecting the KS 20909 data test set (or equivalent) to the 515A data input jack, the KS 20909 output selection must be set to 'Logic near'. In this mode, the data is delivered only to the tip terminal of the data output plug.

```
**************************  CAUTION  **************************
*  To protect against overload, all logic inputs are diode     *
*  clamped to the +5 V supply and to ground. This can cause an *
*  overload to the signal source should the signal level be in *
*  excess of the logic supply voltage or of reverse polarity.  *
*                                                              *
*  To protect the timing signal drivers in the 515A it is      *
*  recommended to limit the current drain to 10 mA on every    *
*  output at all times.                                        *
**************************************************************
```

5.4 ELECTRICAL INTERFACE SPECIFICATIONS

a. 25 position connector and BNC connector
All signals and status leads on these connectors interface with high-speed CMOS logic circuits. When the input signal level is in the range specified below, the input load is purely capacitive (~ 25pF).

State	Level (Volts)
1	+ 5.0 +.2/-1.0
0	0.0 -.2/+1.0

Timing relationships between signals to be provided for implementing the drop-and-insert mode are shown in fig 5.1. In this figure the clock period is 648 ns nominal with a duty cycle of 50% +/- 5%. All signals are delayed with respect to the corresponding clock rising edge by 20 ns nominal.

The clock supplied to the BNC connector must meet the same duty cycle requirement but its frequency can be offset by up to 40 kHz from nominal.

The 4 kb/s input data can change state at any time except in a 200 ns wide region centered around the 4 kHz square wave clock negative going transition.

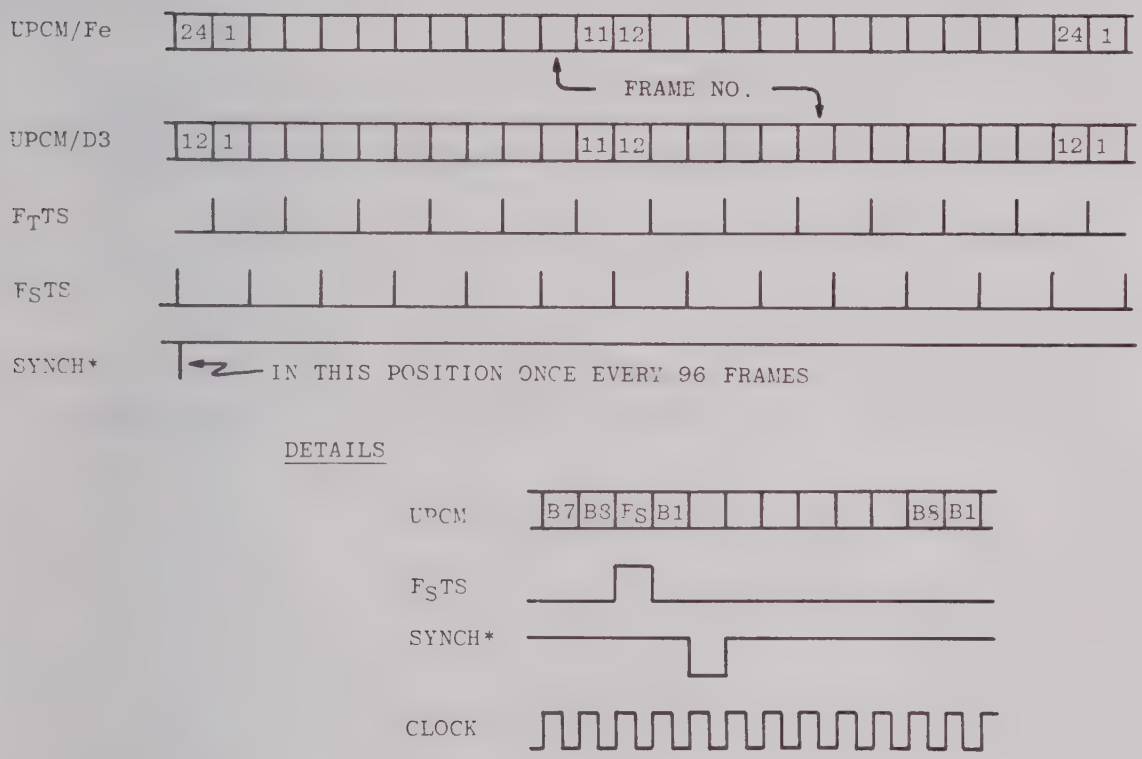


Fig. 5.1 Drop-and-Insert Mode Timing Relationships

b. Option 515A-01 connectors
The signals delivered by the 5 pin connector are provided by a 74LS04 driver. The output logic levels listed below are applicable when the load does not exceed 10 TTLS devices.

The logic input signal presented to the tip and/or ring of the bantam jack drives a TTLS input circuit. The required input logic levels are listed below.

State	Output Level (Volts)	Input Level (Volts)
1	2.4 min	2.0 min
0	0.5 max	0.8 max

Both phases of the 64 kHz and the 8 kHz clocks are provided. The duty cycle of the non-inverted 64 kHz clock is 5/8. The 8

kHz clock non-inverted phase has a duty cycle of 5/64. Fig 5.2 shows the typical timing relationship existing between the clocks and the data supplied by the external source. The data is clocked-in by the negative transitions of the non-inverted 64 kHz clock.

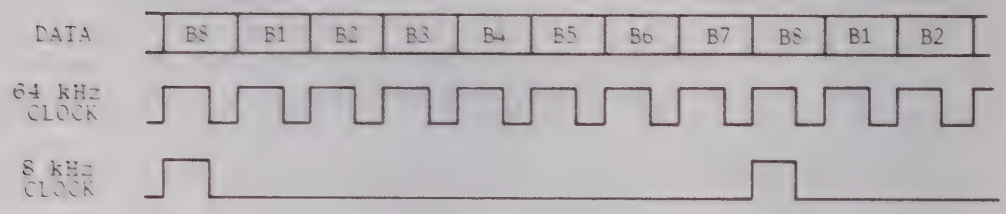


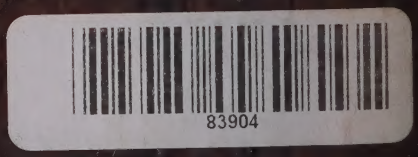
Fig. 5.2 Clock/External Source Timing Relationship

6. ELECTRICAL PERFORMANCE CHECK

This section is in preparation. It will be included in the next issue of the manual, and will also be sent to those from whom T-COM has received the warranty card issued with this manual.

7. MAINTENANCE

This section is in preparation. It will be included in the next issue of the manual, and will also be sent to those from whom T-COM has received the warranty card issued with this manual.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